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COMMON SYSTEMS PROCESSOR FRAME CIRCUIT ARRANGED FOR NO. 2B OR 3 ESS

CHANGES

D. Description of Changes

D.1 Incorporated field modification of the J1C052B-1 (main store controller and main store units) to arrange store-0 for a maximum of two modules of 128K of 18-bit words of memory each, using 16K memory devices as opposed to 4K memory devices. This change is only permitted in No. 3 ESS applications which apply the 3E3 or later issue generic program.

D.2 Added Equipment Note 208 to equipment notes and flag App Figs. 1/1A; Option K in Circuit Notes 102 and 103.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 3615-PK-LEG

COMMON

ELECTRONIC SWITCHING SYSTEMS

COMMON

PROCESSOR FRAME CIRCUIT

ARRANGED FOR NO. 2B AND 3 ESS

CHANGES

D. Description of Changes

D.1 Allowed the use of the ED-4C202-30 and the ED-4C203-30 microprogram store circuit packs. This minimizes the WECo product line and makes available to No. 2B and 3 ESS the extended instruction set.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-DJM-LEG

COMMON

ELECTRONIC SWITCHING SYSTEMS

COMMON

PROCESS FRAME
CIRCUIT

ARRANGED FOR NO. 2B AND 3 ESS

CHANGES

D. Description of Changes

D.1 Changed the microprogram store circuit packs in the 3A CC to save the contents of the store address register and the store controller error register during an initialization. This corrects a complement correction recovery problem. Changed Equipment Note 202 and added Equipment Note 207 to reflect this change.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-DJM-LEG

COMMON SYSTEMS

PROCESSOR FRAME
CIRCUIT
ARRANGED FOR NO. 2B OR 3 ESS

CHANGES

D. Description of Changes

D.1 Added option ZL in Equipment Note 202 to show the new microcode required for No. 2B ESS systems that use the 2B-EF-2 generic program.

D.2 Changed the circuit packs in option ZH of Equipment Note 202 from group 1 to group 2.

D.3 Added Equipment Note 206.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-DJM-LEG

COMMON SYSTEMS

PROCESSOR FRAME CIRCUIT ARRANGED FOR NO. 2B OR 3 ESS

CHANGES

D. Description of Changes

D.1 Replaced 4K-bit memory devices with 16K-bit memory devices for each dual-in-line package (DIP). The higher density memory requires only two memory modules per main store.

D.2 Changed to optional the connection to the additional main store memory units. This allows use of the higher density main store.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-HJA-LEG

COMMON SYSTEMS

PROCESSOR FRAME
CIRCUIT

ARRANGED FOR NO. 2B OR 3 ESS

CHANGES

D. Description of Changes

D.1 Changed power wiring to allow the use of a cost-reduced processor frame power unit (8-ampere version).

D.2 Added two options:

(a) Option ZE for the non-cost-reduced (4-ampere) power unit (rated Mfr Disc.)

(b) Option ZF for the cost-reduced (8-ampere) power unit (rated AT&T Co Standard)

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-DJM-LEG

COMMON SYSTEMS PROCESSOR FRAME CIRCUIT ARRANGED FOR NO. 2B OR 3 ESS

CHANGES

B. Changes in Apparatus

B.1 Added

R13 and R14 resistors KS-16645,L2, 1 KOHM - App Figs. 2 and 2a

D. Description of Changes

D.1 Added R13 and R14 termination resistors to suppress noise generated on the 3A central control (CC) switch scan leads.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5435-DJM-LEG

COMMON SYSTEMS PROCESSOR FRAME CIRCUIT ARRANGED FOR NO. 2B OR 3 ESS

CHANGES

D. Description of Changes

D.1 Showed connections for teletypewriter (TTY) controllers 4 and 6 for No. 3 ESS.

D.2 Added options ZA, ZB, ZC, and ZD to show the interrupt connections for TTY controllers 4 and 6 in No. 3 ESS systems. These options allow TTY controllers 4 and 6 to individually use either the normal TTY even interrupt or interrupt bit 12.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5435-DJM-LEG

COMMON

PROCESSOR FRAME
CIRCUIT
ARRANGED FOR NO. 2B OR NO. 3

CHANGES

D. Description of Changes

D.1 Added options J. G, ZG, and ZH, which show the use of microprogram store circuit packs with 512 of 1024 words per pack. Options J and G (rated A & M Only) are for packs with 512 words. Options ZG and ZH (rated Standard) are for boards with 1024 words.

D.2 Allowed the removal of up to four power converters in the processor frame power unit, when using microprogram store circuit packs with 1024 words per pack.

D.3 Added two options:

(a) Option F (rated A & M Only) to show the use of microprogram store packs with 512 words per pack.

(b) Option E (rated Standard) to show the use of 1024 boards.

D.4 Added options B and A, which show the wiring necessary when using cost-reduced backplanes for the main memory. Option B (rated A & M Only) is for the ED-4C005-30 backplane. Option A (rated Standard) is for the new ED-4C091-30 backplane.

COMMON SYSTEMS

PROCESSOR FRAME
CIRCUIT
ARRANGED FOR NO. 2B OR 3 ESS

CHANGES

D. Description of Changes

D.1 Added a capacitor to net PWRØFF0 to prevent random initializations.

D.2 Removed the store busy signal between 3A CCs.

D.3 Changed Equipment Note 202 to reflect microprogram store changes.

D.4 Showed connections for TTY controllers 2 and 3 for No. 3 ESS.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5435-DJM-LEG

CIRCUIT DESCRIPTION

CD-1C910-02
ISSUE 1
DWG ISSUE 1
DISTN CODE 7N98

COMMON SYSTEMS

PROCESSOR FRAME
CIRCUIT

ARRANGED FOR NO. 2B OR 3 ESS

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The processor frame provides for the housing and interconnection of the various equipment units that comprise the system control units (CUs). The following equipment is included in the CU:

(a)	ED-5A120-10,G3	Frame Filter
(b)	J1C057A-1	Processor Frame Power Unit
(c)	J1C050A-1	3A Central Control
(d)	J1C052B-1,L1	Main Store Controller and Memory Unit
(e)	*J1C052B-1,L3	Main Store Memory Unit(s)
(f)	*J2H121AA-1	I/O Unit
(g)	*J2H121AB-1	I/O and Bus Termination Unit
(h)	*J2H121AC-1	Terminal Strip

2. GENERAL DESCRIPTION OF OPERATION

2.01 The double-bay processor frame accommodates duplicated CUs. The active CU controls the overall office operations while the inactive CU remains in a standby state. Each bay is powered from a separate power bus.

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* Optional

2.02 The main store (MAS) units provide up to 256K words of stored program to direct the 3A central control (3A CC) through its sequences. The I/O units provide parallel access to the No. 2B peripheral.

SECTION II - DETAILED DESCRIPTION

1. FRAME POWER - FS 1

1.01 The +24 volt and -48 volt potentials of the office are bused independently to each bay of the double-bay processor frame. Power circuits for bay 0 are shown on sheets B1AA, B1AB, and B1AC. Sheets B1AD, B1AE, and B1AF show the power circuits for bay 1. A local filter is provided in each bay for the +24 volts. The return associated with +24 volts is grounded at the processor frame and the -48 volt return lead is floating at the processor frame and is grounded at the office power distribution point.

1.02 A processor frame power unit (PFPU) provides fusing and further distribution of the +24 volts and -48 volts in each bay. The PFPU also provides for the generation of +3 volts and +5 volts for the 3A CC. The power potentials required by the MAS and I/O units are contained in the MAS and I/O units. The power switch on the 3A CC control panel, in conjunction with the PFPU, controls the on-off state of CU power except that it does not control the +24 volts and -48 volts associated with power generation and control. Refer to the processor frame power circuit (PFPC) description for the details of power control.

1.03 Two levels of power related alarms are generated in the CU. Fuse alarms and power converter FA signals are detected by the PFPU and converted into a major alarm. Converter power alarm (PA) signals result in a frame minor alarm. The FA signal indicates a power loss and results in a shutdown of remaining power in the affected CU. The PA signal indicates an out-of-tolerance condition of a power converter. The PA signal from a +5 volt converter supplying MAS circuits is converted into an FA signal at the MAS so that all power will be removed from the memory as soon as its +5 volt power is out of tolerance.

1.04 The CVFA1 net links the CU power converter FA signals to the detector circuit in the PFPU. Composite diagram 1 shows how this net is combined with the CVFA1Z net to pick up the I/O unit converters when the I/O unit is equipped. The FA1Z and NPA2 nets also run throughout the CU to connect all power converter PAT and NPA terminals. These connect to the PAT02 and the NPA02 nets connect to the I/O unit as shown in composite diagram 1.

1.05 A power alarm test insures the ability of each power converter in the CU to generate a PA signal that will be detected by the PFPC. Much of the converter FA circuitry is common to its PA circuitry, thus increasing the probability of this signal functioning properly. Refer to the PFPC description for a detailed operation of the test. Composite diagram 2 illustrates the unique wiring of the PA net required by this test. To verify that the PA net is wired to each converter, it is wired in a series loop from converter to converter. A continuity check of the loop is made as part of the power alarm test. A voltage source is connected to one end of the net via the PAT relay contact. This voltage is passed over lead PA01 to each J87422A power converter in the memory unit, through the operated K1 relay on circuit pack FC262 (K1 is operated during the test) to lead PA121. Lead PA121 picks up the PA terminal of the +5 volt converter in the PFPU that supplies memory termination circuit power (PM039A). The net continues from PM039A via STCVPA1, which connects to the +5 volt converter (J87421A) in each memory unit, and via circuit pack FC262, appears on PA041 to the PA terminal of circuit pack FB152 in the 3A CC. If the I/O unit is not equipped, the PA net returns to the PFPU from the 3A CC on net PA1. If the I/O unit is equipped, PA051 extends the PA net to it so the power converters can be picked up before being returned to the PFPU on PA1.

1.06 At the PFPU, PA1 loops to each power converter PA terminal. PASMAS1 extends the PA net to the supplementary main store (SMAS) frame (if one is equipped). PASMAS1 loops to the PA terminal of all power modules in the SMAS and is returned to the PFPU on PAI1. PASMAS1 connects directly to PAI1 at the PFPU when there is no SMAS frame. PAI1 connects to the minor alarm flip-flop in the PFPU. Thus, the voltage applied to PA01 by the operation of the PAT relay is looped to each PA terminal in the CU and terminates at the minor alarm flip-flop, where its presence sets the alarm state to verify the continuity of the PA net.

2. STORE BUS - FS 2

2.01 Each 3A CC has access to its associated memory and the memory associated with the other 3A CC. (See sheets B2AA and B2AB.) Memory is equipped in stores of up to 256K words. Each store can be partially equipped in units of 64K words. The main store controller and memory (MASCM) unit contains control circuitry and the first 64K words of memory for a store. Up to three main store memory (MASM) units are added to provide the additional words per store. The first store 0 is equipped in

the processor frame. Additional stores are equipped in the SMAS frames.

2.02 Address, data, and control signals are passed between the 3A CC and memory units. The 3A CC communicates directly to its associated basic MASCM unit (ie, the one in the processor frame). The appropriate signals are grouped at the 3A CC as element MAS0, MASCM, and MASBUS (elements are preceded with 0 or 1 for bay 0 or 1, respectively). Repeaters in the basic MASCM unit interface these signals to the growth memory blocks. These signals are grouped in the MASCM element GMASBUS.

2.03 The 3A CC communicates with the other memory via the other 3A CC. Signals between 3A CC 0 and memory 1 are grouped at 0STOBUS1 and connect to 3A CC 1 at 1STOBUS0. These are connected to memory 1 via the 1MAS0/1MASBUS connection. Signals between 3A CC 1 and memory 0 are grouped at 1STOBUS1 and connect to 3A CC 0 at 0STOBUS0. They are connected to memory 0 via the 0MAS0/0MASBUS ports. These data paths are shown in detail for address bit 0 and data bit 0 in composite diagram 1 and composite diagram 2 as representative of other connections.

2.04 Referring to composite diagram 1, memory address bit 0 resides in the 3A CC store address register (SAR) on lead SAR0. When the 3A CC 0 desires to access its own memory, lead REQS0I0 is active and directs the state of SAR0 to lead 0SA00000 via 0MAS0. 0MASBUS forwards the signal to circuit pack FA1060 in the MASCM unit where it is directed to the address inputs of the memory. The MASCM also repeats the signal to other memory blocks on lead 0SA20000 via 0GMASBUS.

2.05 When the 3A CC 0 desires to access the other store, lead REQS1I0 is active. The SAR0 state thus appears on 0SA10000 via 0STOBUS1 to 1STOBUS1. The 3A CC 1 forwards the signal on lead 1SA00000 to the MASCM unit for the first block of memory associated with 3A CC 1. The MASCM unit delivers the signal to its memory address inputs and forwards the signal to its associated growth stores via 1SA20000.

2.06 The signal path for data bit zero, shown in composite diagram 2, is similar to that described for the address bit. The points being connected are the 3A CC store data register (SDR) and the memory data bits. The flow of data in this case is bidirectional - from the 3A CC to the memory for a write function and from the memory to the SDR for a read function.

3. MEMORY - FS 3

3.01 Sheets B3AA and B3AB show the frame connection between memory units. The address, data, and control signals are bused from the MASCM unit to the first MASM unit when it is equipped and from each MASM unit to successive MASM units as they are equipped. Terminating circuits are required on address and data leads to insure signal fidelity. These are equipped on the last memory unit. Thus, options allow for the equipping of the terminations on the MASCM unit or on any of the MASM units, depending on the size of the memory. Note that the lead mnemonics are preceded with 01, 02, 03 or 04 as an indication of the level of cabling. Level 01 signals emanate from the MASCM unit and level 02 signals emanate from the first MASM unit, etc.

3.02 A MASM unit can be equipped as either the second, third, or fourth 64K words of a memory block. Connections are specified at the frame level to identify the MASM as the proper unit. These are the 0/1M*SL__A/B (where * = 2, 3, 4, 5, 6 or 7 and __ = 00, 01, 10,....,21) mod select leads.

4. I/O - FS 4

4.01 Sheets B4AA and B4AB show the I/O associated connections for bay 0 and bay 1. The 3A CC sends parallel data from its general registers 9 and 10 along with timing and control signals from element 0/1CCMANCH to the I/O unit element 0/1I/OLOG. The I/O unit returns parallel data from its IOD register and control flags to the 3A CC. (0/1I/OLOG is required for No. 2 ESS and is not required for No. 3 ESS.)

4.02 Data is exchanged in serial format between the 3A CC and its peripheral units including the MASCM units, teletypewriter controllers (TTYCS), tape data controllers (TDC), and the system status panel controller, all of which are controlled by subchannels of main channel 0 as shown in Information Note 303. Other peripheral units can be assigned to main channel 1 as required by the system.

4.03 Interrupt signals to the 3A CC are required for operation of the TTYCs and TDCs for No. 3 ESS. They connect to 0/1INTRPT. No. 2 ESS functions with these units on a timed, rather than demand, interrupt basis and does not require the interrupt connections.

5. 3A CC MAINTENANCE CHANNEL - FS 5

5.01 The maintenance channel links each 3A CC of a duplex system for diagnostic purposes. It is a two-way ac coupled link employing serial data communication.

6. 3A CC SYSTEM STATUS PANEL - FS 6

6.01 In addition to the serial I/O channel connection between the 3A CC and the system status panel controller, a

dedicated ac data path exists between the panel and each 3A CC to allow the 3A CC to be forced on line and to be initialized.

7. I/O UNIT - FS 7

7.01 Central pulse distributor (CPD), peripheral unit address bus (PUAB), scan answer bus (SAB), dial pulse seize and release, and data bus connections to the No. 2 ESS periphery are shown in FS 7. FS 7 is not required for No. 3 ESS.

8. MAIN MEMORY TERMINATION - FS 8

8.01 FS 8 shows the memory terminating circuits.

9. UNIT SELECT CONNECTIONS - FS 9

9.01 Frame wiring required to define the 3A CC units in bay 0 and bay 1 is shown in FS 9 (eg, 3A CC 0 and 1, respectively, and the MASCM units in each bay as MASCM unit 00).

10 CC INTERRUPT OPTIONS - FS 10

10.01 This FS shows the 3A CC connections required to define 5-ms and 10-ms interrupt signals. The 5-ms interrupt signal is required for No. 2 ESS and the 10-ms interrupt signal is required for No. 3 ESS.

11. ANSWER BUS TERMINATIONS - FS 11

11.01 FS 11 shows the connection of terminating resistors to the SAB leads for No. 2 ESS.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 Provides filtering of the +24 volt office battery for the units equipped on the frame.

3.02 Provides for housing and interconnection of equipment that comprises the system processor.

3.03 Provides a reference point for connection to other frames in the system.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon should be followed.

4.02 The following circuits are (may be) equipped on the processor frame and are included as connecting circuits:

(a) 3A Central Control
Circuit - SD-1C900-01.

(b) 3A Central Control - Control Panel
Circuit - SD-1C901-01.

(c) Main Store Controller
Circuit - SD-1C902-02.

(d) Main Store Memory
Circuit - SD-1C903-02.

(e) Processor Frame Power
Circuit - SD-1C911-01.

(f) 2B ESS I/O Control
Circuit - SD-2H099-01.

4.03 Additional connecting circuits depend on the system application for this common systems frame. The following circuits are representative:

(a) Maintenance Frame
Circuit - SD-1C912-01.

(b) Communication Bus
Circuit - SD-2H078-01.

(c) Control Frame Circuit - SD-3H902-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements for this common systems frame are determined by the using system. X-78890 specifies the manufacturing testing requirements for the No. 2B ESS processor which includes this frame.